REMARKS

Claims 1-20 are all the claims pending in the application.

New claim 21 has been added to provide additional coverage for Applicant's invention.

The Examiner has rejected claims 1-4, 7-10, 11-14 and 17-20 under 35 U.S.C. § 103(a) as being unpatentable over Baxter et al. and Kolchinsky. Applicant traverses these rejections because the cited references fail to disclose or suggest all of the claim limitations. Specifically, the references fail to disclose or suggest at least the following limitations of independent claims 1 and 11:

> executing digital image processing of an interval of active pixel in the condition that a first internal logic description is written in said field programmable gate array;
>
> executing digital control processing in the condition that said first internal logic description of said field programmable gate array is rewritten to a second internal logic description in an interval of non-active pixel with the exception of said interval of active pixel; and
>
> executing digital image processing again in the condition that said second internal description is rewritten to said first internal logic description;

Applicant first notes that the Examiner concedes that Baxter et al. fails to disclose a field programmable gate array (FPGA) for executing the image and control processing wherein the first and second internal logic descriptions, corresponding to each type of processing, are written to the FPGA. Instead, the Examiner asserts that Baxter et al. discloses using dedicated processors 66 and 70 for executing each type of processing.

In order to make up for this deficiency, the Examiner cites to Kolchinsky. Specifically, the Examiner asserts that Kolchinsky discloses a reconfigurable image processing system (figure

2) that is implemented by case address generator 22 and arithmetic unit 26 (see figure 2), wherein arithmetic unit 26 operates to process image data.

However, Kolchinsky does not disclose that the arithmetic unit 26 performs processing in the time sequence (active pixel interval, non active pixel period, active pixel period) required by the claim. For example, claim 1 requires that image processing is performed in the FPGA, then control processing is performed and then the same image processing is preformed again.

Regarding claims 2-4, 7-10, 12-14 and 17-20, they should be allowable at least based on their dependence from claims 1 or 11 for at least the same reasons.

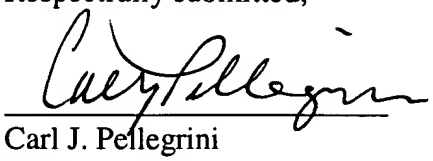
Regarding claims 5, 6, 15 and 16, which have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Baxter et al. and Kolchinsky, and further in view of Fukuoka, they should be allowable at least based on their dependence from claims 1 or 11 for at least the same reasons.

Regarding new claims 21 and 22, they should be allowable at least for the same reasons as claims 1 and 11. In addition, claim 21 requires that the control processing is pre-processing or post-processing relating to said image processing. Claim 22 also requires that the control and image processing occur in the same frame. Neither of these limitations are disclosed or suggested in the cited references.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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